METHOD FOR OPTIMIZATION OF LOGIC CIRCUITS FOR ROUTABILITY IMPROVEMENT

ABSTRACT OF THE DISCLOSURE

Routability (or wiring congestion) in a VLSI chip is becoming increasingly important as chip complexity increases. Congestion has a significant impact on performance, yield, and chip area. The present invention targets the optimization of congestion early in technology independent synthesis prior to physical design.

Instead of attempting to optimize the logic structure as well as the spatial placement of a circuit, we pose a more modest goal limiting such optimization to the scope of logic synthesis. That is, we propose an aggressive optimization approach that is cognizant of circuit structure during technology independent synthesis and produces more predictable implementations which give better routability and yield.